



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#4/Amend A  
6.5.02  
C. Wills

In re application of:

K. Gotoh et al.

Art Unit: Not Assigned

Application No.: 10/082,055

Examiner: Not Assigned

Filed: February 26, 2002

Atty. Dkt. No.: 100021-00074

For: TEST CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT EFFECTIVELY  
CARRYING OUT VERIFICATION OF CONNECTION OF NODES

**PRELIMINARY AMENDMENT**

Commissioner for Patents  
Washington, D.C. 20231

Date: June 3, 2002

Sir:

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JUN -4 2002  
TC 2800 MAIL ROOM

Prior to initial examination of the application, please amend the above-identified application as follows:

**IN THE DRAWINGS:**

A Request for Approval of Drawing Corrections, with proposed changes to Figure 6 highlighted in red is attached hereto.

**IN THE CLAIMS:**

Please amend claims 41 and 43 as follows. A marked-up version of the claims is attached hereto.

41. (Amended) A test circuit that is incorporated in a device having an input circuit for inputting a signal, and that carries out a verification of a connection of nodes of said device, said test circuit comprising:

a test data generating circuit processing test data for carrying out a verification of a connection of input nodes of said input circuit; and

a test input buffer, connected in parallel with said input nodes, receiving test data from said input nodes and inputting the test data to said test data processing circuit.

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